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Information technology — Telecommunications and information exchange between systems — Near Field Communication Wired Interface (NFC-WI)

Technologies de l'information — Téléinformatique — Interface câblée de communication de champs proche (NFC-WI)

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Contents

Page

Foreword ... iv

Introduction ... v

1 Scope ... 1

2 Terms and definitions ... 1

3 Conventions and notations ... 1
3.1 Representation of bit values ... 1
3.2 Representation of logical states of LOW and HIGH ... 1
3.3 Capitalisation of names ... 2
3.4 State notation ... 2

4 Symbols and abbreviated terms ... 2

5 General ... 2

6 Signals ... 3
6.1 Signal wires ... 3
6.2 Electrical characteristics ... 3
6.3 Clock frequency (f_{CLK}) ... 4

7 NFC-WI states ... 4
7.1 Off state ... 5
7.2 Activating state ... 5
7.3 On state ... 7
7.4 De-Activating state ... 8
7.5 Command state ... 9

8 Information-transfer ... 10
8.1 Manchester bit coding ... 10
8.2 Modified Miller bit coding ... 10
8.3 Bit coding for f_{CLK}/128 (~106 kb/s) ... 11
8.4 Bit coding for f_{CLK}/64 (~212 kb/s) ... 11
8.5 Bit coding for f_{CLK}/32 (~424 kb/s) ... 12

Annex A (informative) **Application of NFC-WI with NFCIP-1** ... 13

Annex B (informative) **Command state configuration** ... 17

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Foreword

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Introduction

Following the standardisation of Near Field Communication (NFC) systems and their test methods in Ecma International, this International Standard specifies a two-wire interface between two components called “Transceiver” and “Front-end”. Systems that implement the NFC-WI interface can thus be augmented with, for example, a wireless Front-end for NFCIP-1 as illustrated in Figure 1. Although this International Standard only specifies requirements for the Signal-In and Signal-Out wires and the digital signals they carry, informative Annex A lists some NFCIP-1 specific considerations.

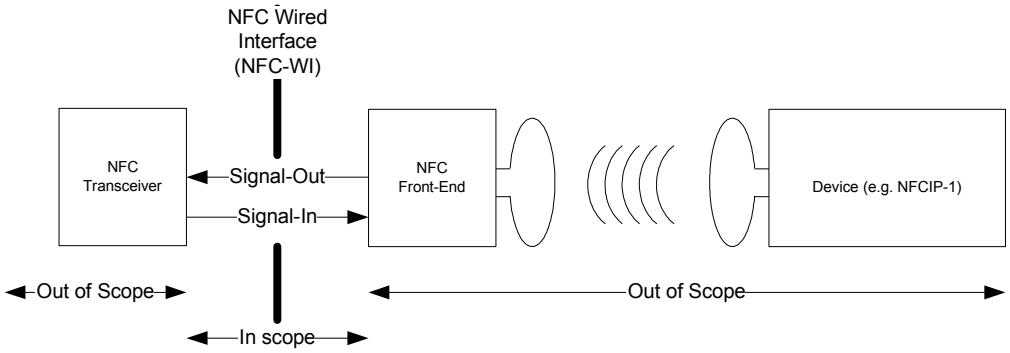

Figure 1 — Context diagram for the NFC wired interface

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Information technology — Telecommunications and information exchange between systems — Near Field Communication Wired Interface (NFC-WI)

1 Scope

This International Standard specifies the digital wire interface between a Transceiver and a Front-end. The specification includes the signal wires, binary signals, the state diagrams and the bit encodings for three data rates.

2 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

2.1
Clock
sequence of LOW and HIGH as defined in 3.2 with duration of $1/(2*f_{CLK})$, where f_{clk} is the clock frequency as defined in 6.3

2.2
Information
bit-coded data as defined in Clause 8

2.3
Front-end
entity that drives the Signal-Out wire and receives on the Signal-In wire

2.4
Transceiver
entity that drives the Signal-In wire and receives on the Signal-Out wire

3 Conventions and notations

3.1 Representation of bit values

Bit values are either ZERO or ONE.

3.2 Representation of logical states of LOW and HIGH

— The logical signal state is LOW if the electrical level of a signal has the input voltage of V_{IL} or the output voltage of V_{OL} as specified in Table 1 in 6.2.

— The logical signal state is HIGH if the electrical level of a signal has the input voltage of V_{IH} or the output voltage of V_{OH} as specified in Table 1 in 6.2.

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3.3 Capitalisation of names

The initial character of names of basic elements, e.g. specific fields, is capitalised.

3.4 State notation

The states are specified in Unified Modelling Language (UML) notation.

4 Symbols and abbreviated terms

AND	Logical AND operation
f_{CLK}	Clock frequency as defined in 6.3
NFC-WI	Near Field Communication Wired Interface
OR	Logical OR operation
XOR	Logical XOR operation
÷	Divide a clock frequency by a constant value.

Table 1 in 6.2 list additional symbols for electrical characteristics.

5 General

The NFC-Wired Interface (NFC-WI) specifies the Signal-In and the Signal-Out wires as illustrated in Figure 2. The wires carry binary signals of HIGH and LOW.

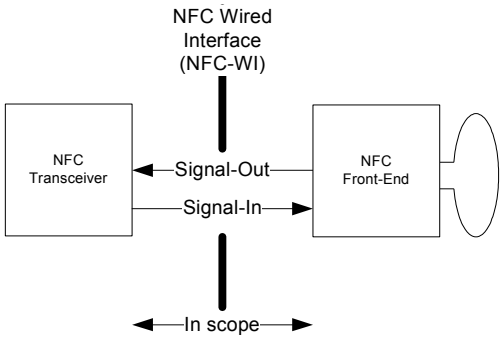

Figure 2 — NFC-WI

The combinations of the signals on the wires make up the NFC-WI states as defined in Clause 7.

Clause 8 specifies encodings for Information transfer, while in the On state, for the $f_{CLK}/128$, $f_{CLK}/64$ and $f_{CLK}/32$ data transfer rates.

Annex A lists NFCIP-1 specific considerations for implementing the NFC-WI; Annex B lists possible uses of the Command state, such as changing to alternative protocols.

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6 Signals

6.1 Signal wires

6.1.1 Signal-In

The Transceiver drives the Signal-In wire with a binary signal of HIGH and LOW. The Front-end receives the binary signal on Signal-In.

6.1.2 Signal-Out

The Front-end drives the Signal-Out wire with a binary signal of HIGH and LOW. The Transceiver receives the binary signal on Signal-Out.

6.2 Electrical characteristics

The wires shall carry (binary) digital signals as illustrated in Figure 3 and specified in Table 1.

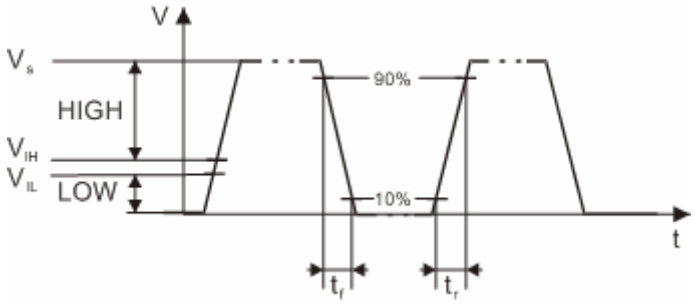

Figure 3 — Illustration of some electrical parameters

Table 1 — Electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
DC Characteristics					
V_S	Signalling voltage amplitude	Not applicable	1,62	3,63	V
V_{IH}	HIGH level input voltage	Not applicable	1,10	3,63	V
V_{IL}	LOW level input voltage	Not applicable	0	0,70	V
I_{LI}	Input leakage current	Input voltage is between V_{ILmin} and V_{IHmax}		± 4	mA
V_{OH}	HIGH level output voltage	Driver source current of 4mA	1,32	3,63	V
V_{OL}	LOW level output voltage	Driver sink current of 4mA	0	0,30	V

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AC Characteristics					
t_r	Signal-In, Signal-Out rise time (from 10 % to 90 % of V_S)	Add an external capacitive load between 10 pF and 30 pF for testing	4	20	ns
t_f	Signal-In, Signal-Out fall time (from 90 % to 10 % of V_S)	Add an external capacitive load between 10 pF and 30 pF for testing	4	20	ns
t_{SP}	Pulse width of spikes and glitches which must be suppressed by the input filter	Not applicable		1	ns
C_I	Input capacitance	1 MHz test frequency		10	pF
C_L	External load capacitance for the driver	Not applicable		30	pF
V_{ITR}	Input voltage range at signal transitions	Not applicable	− 0,30	3,93	V
	Pulse width	Not applicable	30		ns
Environmental/Test Conditions					
T_{amb}	Ambient temperature for electrical characteristics measurements	Not applicable	20	26	°C

6.3 Clock frequency (f_{CLK})

The clock frequency (f_{CLK}) shall be 13,56 MHz ± 7 kHz.

7 NFC-WI states

Figure 4 specifies the main NFC-WI states.

The Off state and the On state are the main NFC-WI states. The Off state is the default state.

NFC-WI shall move from the Off state to the On state as specified in 7.2.

NFC-WI shall move from the On state to the Off state as specified in 7.4.

NFC-WI shall move from the On state to the Command state via the Escape sequence.

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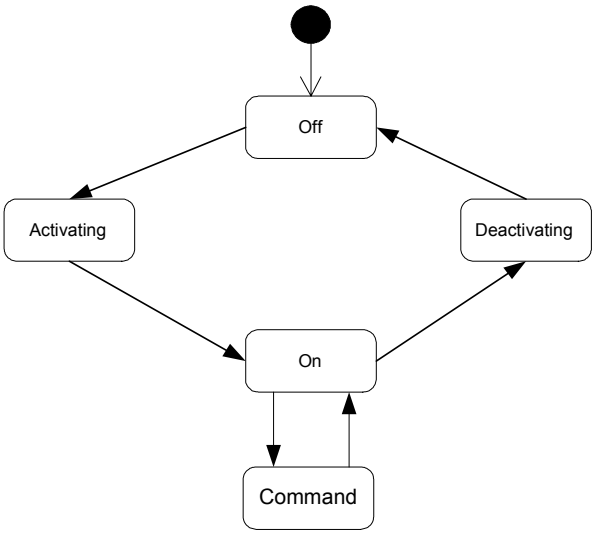

Figure 4 — Main states of NFC-WI

7.1 Off state

When Signal-In and Signal-Out are LOW for at least 120 µs, the NFC-WI state shall be Off.

NOTE In this state, power saving features may be implemented.

7.2 Activating state

The NFC-WI shall enter the Activating state when either Signal-Out or Signal-In carry the activation sequence, as specified in 7.2.1 and 7.2.2 respectively. When subsequently the opposite wire carries the activation response, the NFC-WI shall enter the On state, as shown in Figure 5.

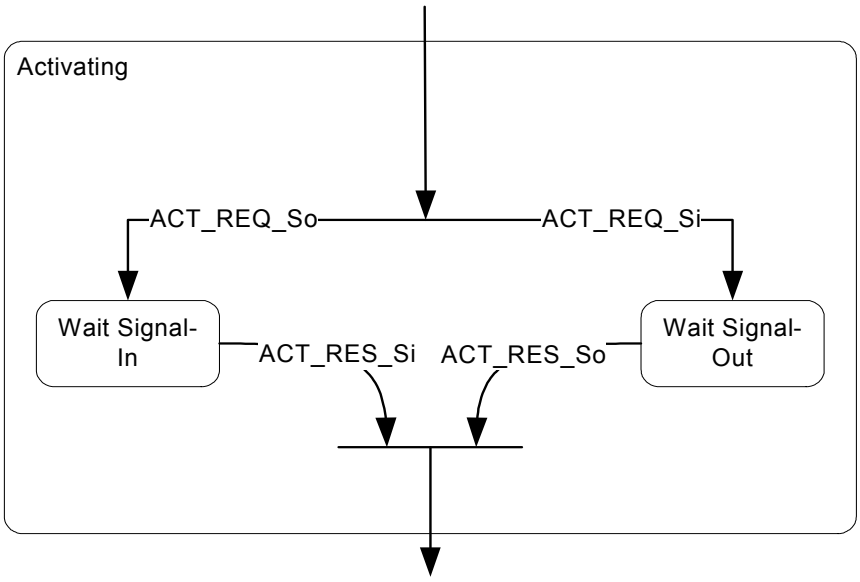

Figure 5 — Activating state

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7.2.1 Signal-Out activation

When the Signal-Out wire carries the ACT_REQ_So, the NFC-WI shall enter the Activating state. When Signal-In carries the ACT_RES_Si no later than 50 ms after entering the Activating state the NFC-WI shall enter the On state. Otherwise the NFC-WI shall enter the Off state.

The activation sequence is illustrated in Figure 6 and Figure 7.

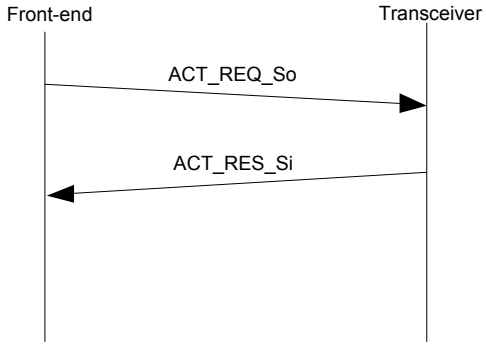

Figure 6 — Signal-Out activation

7.2.1.1 ACT_REQ_So

The Clock on the Signal-Out wire constitutes the ACT_REQ_So as illustrated in the upper part of Figure 7.

7.2.1.2 ACT_RES_Si

The HIGH on Signal-In constitutes the ACT_RES_Si as illustrated in the lower part of Figure 7.

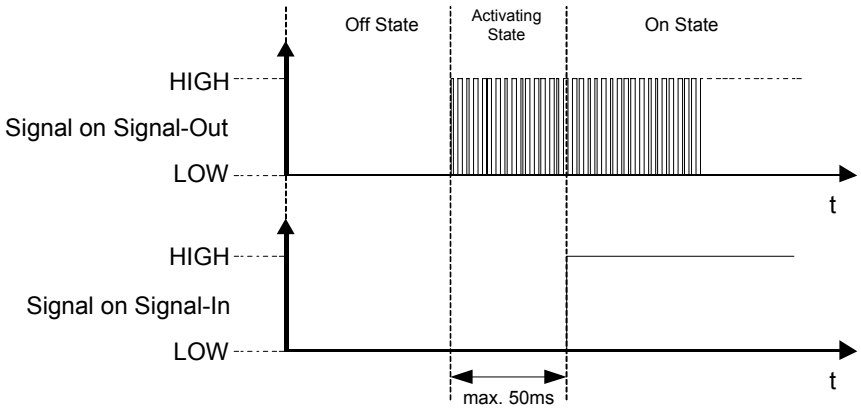

Figure 7 — Signal-Out initiated activation sequence

7.2.2 Signal-In activation

When the Signal-In wire carries the ACT_REQ_Si, the NFC-WI shall enter the Activating state. When Signal-Out carries the ACT_RES_So within a period of between 100 µs and 50 ms after entering the Activating state the NFC-WI shall enter the On state. Otherwise the NFC-WI shall enter the Off state.

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The activation sequence is illustrated in Figure 8 and Figure 9.

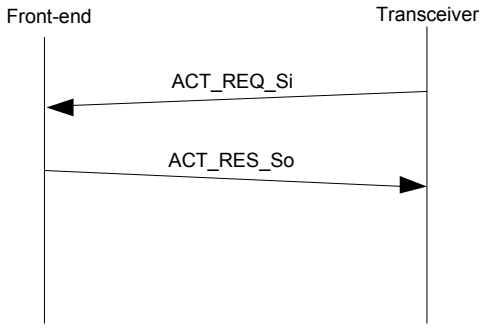

Figure 8 — Signal-In activation

7.2.2.1 ACT_REQ_Si

At least 127 pulses with a frequency in the range of 2 MHz to 12 MHz on Signal-In constitute the ACT_REQ_Si as illustrated in the upper part of Figure 9. Subsequently Signal-In shall be HIGH.

7.2.2.2 ACT_RES_So

The Clock on the Signal-Out wire constitutes the ACT_RES_So as illustrated in the lower part of Figure 9.

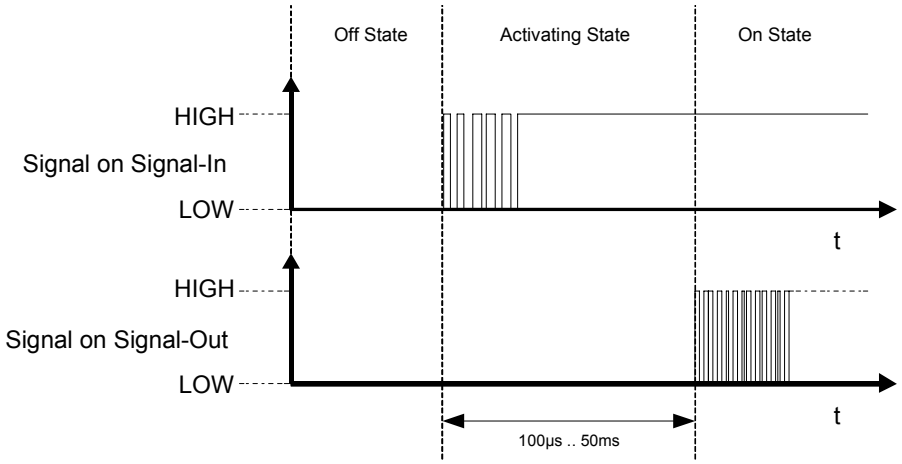

Figure 9 — Signal-In initiated activation sequence

7.3 On state

The On state consists of the Idle and Busy sub states; Idle is the default sub-state of On, as shown in Figure 10.

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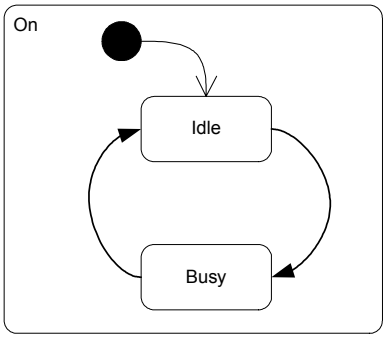

Figure 10 — The On state

7.3.1 Idle

While in the On state, in the absence of Information-transfer, the On sub-state shall be Idle. In the Idle sub-state, Signal-In shall carry HIGH, and Signal-Out shall carry the Clock.

7.3.2 Busy

While in the On state, during Information-transfer on either Signal-In or Signal-Out, the On sub-state shall be Busy.

7.4 De-Activating state

The NFC-WI shall enter the De-Activating state when either Signal-Out or Signal-In carry the deactivation sequence as specified in 7.4.1 and 7.4.2 respectively. When subsequently the opposite wire carries the deactivation response, the NFC-WI shall enter the Off state, see Figure 11.

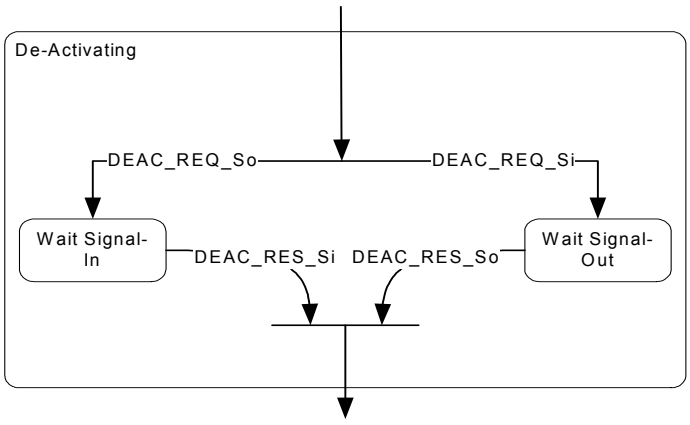

Figure 11 — De-Activating state

7.4.1 Signal-Out deactivation

When Signal-Out carries DEACT_REQ_So, the NFC-WI shall enter De-Activating state. Within 50 ms, the Signal-In shall carry DEACT_RES_Si, and the NFC-WI shall enter the Off state.

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7.4.1.1 DEACT_REQ_So

Signal-Out set to LOW for more than 120 µs constitutes the DEACT_REQ_So.

7.4.1.2 DEACT_RES_Si

Signal-In set to LOW constitutes the DEACT_RES_Si.

7.4.2 Signal-In deactivation

When Signal-In carries DEACT_REQ_Si, the NFC-WI shall enter De-Activating state. Within 50 ms, the Signal-Out shall carry DEACT_RES_So, and the NFC-WI shall enter the Off state.

7.4.2.1 DEACT_REQ_Si

Signal-In set to LOW for more than 120 µs constitutes the DEACT_REQ_Si.

7.4.2.2 DEACT_RES_So

Signal-Out set to LOW constitutes the DEACT_RES_So.

7.5 Command state

The Command state shall be entered from the On state using the Escape sequence. The default bit coding in Command state shall be as defined in 8.3, Bit coding for $f_{CLK}/128$.

The Command state is exited with a command. The command set is outside the scope of this International Standard.

7.5.1 Escape sequence

At least 127 pulses with a frequency in the range from 2 MHz to 12 MHz on Signal-In constitute the Escape sequence as illustrated in Figure 12. Subsequently Signal-In shall be HIGH.

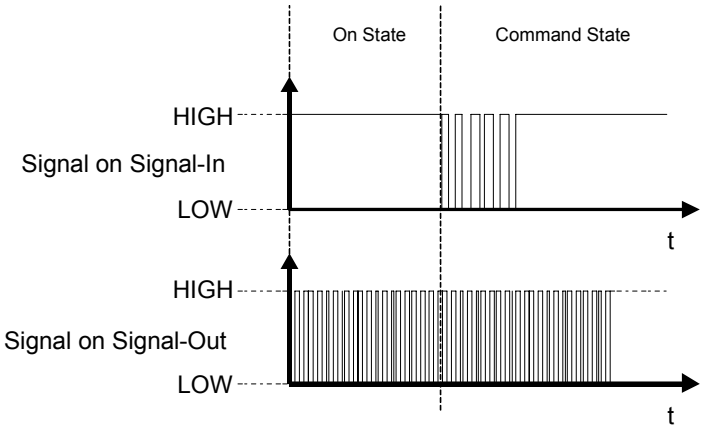

Figure 12 — Escape sequence

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8 Information-transfer

This Clause specifies the bit coding for three data rates.

8.1 Manchester bit coding

The Manchester bit coding encodes ONE and ZERO in a LOW to HIGH transition in the middle of a bit period as illustrated in Figure 13.

The first half of the bit is HIGH and the second half of the bit is LOW for a ONE.

The first half of the bit is LOW and the second half of the bit is HIGH for a ZERO.

Reverse polarity shall be permitted.

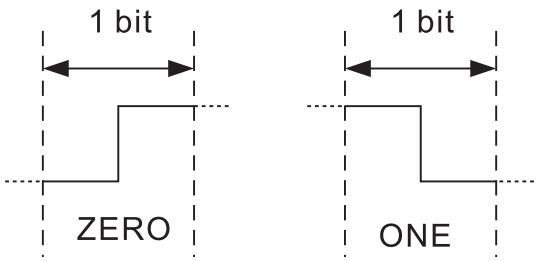

Figure 13 — Manchester bit coding

8.2 Modified Miller bit coding

The Modified Miller bit coding defines ONE and ZERO by the position of a pulse during one bit period. The pulse is a transition from HIGH to LOW, followed by a period of LOW, followed by a transition to HIGH. The bit representation is illustrated in Figure 14.

For a ONE the pulse shall occur in the second half of the bit period; the transition from HIGH to LOW shall be in the middle of the bit period.

For a ZERO a pulse shall occur at the beginning of the bit period with the following exception. In case a ZERO bit follows a ONE bit, no pulse shall occur during this ZERO.

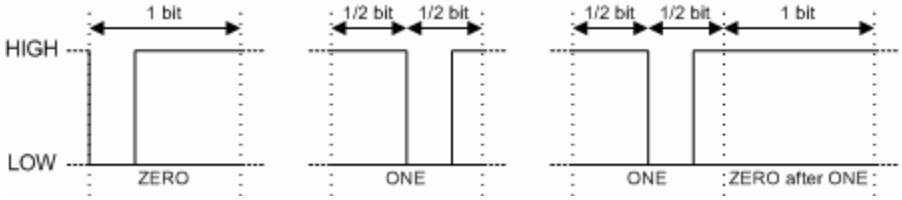

Figure 14 — Modified Miller bit coding

The jitter margin for the rising pulse edge is +/- 2/*fc*.

NOTE For implementation recommendations the propagation delays as specified in A.3 should be respected.

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8.3 Bit coding for $f_{CLK}/128$ (~106 kb/s)

8.3.1 Signal-Out

Signal-Out shall carry the AND combination of the Modified Miller bit coded data and f_{CLK} as illustrated in Figure 15.

The Modified Miller bit coded pulse is at least 7 and at most 45 f_{CLK} cycles long.

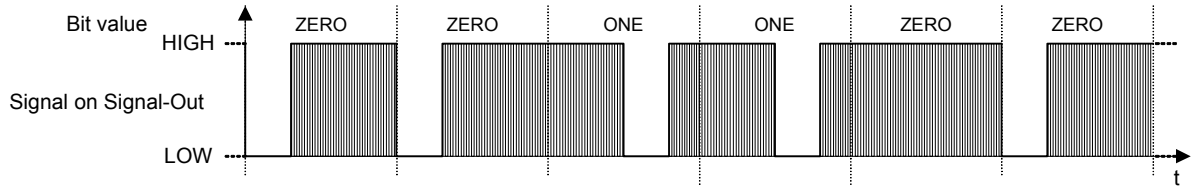

Figure 15 — Signal-Out coding at $f_{CLK}/128$

8.3.2 Signal-In

Coding on Signal-In shall carry the OR combination of the inverted Manchester bit-coded data and (f_{CLK}÷16). Every bit shall start with the low phase of the (f_{CLK}÷16) as illustrated in Figure 16.

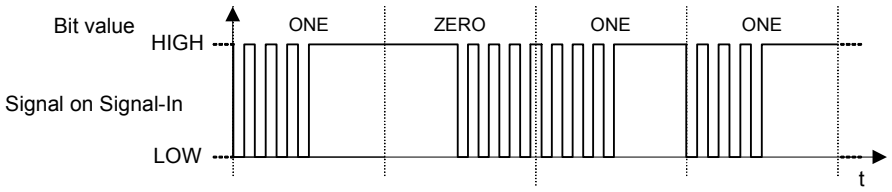

Figure 16 — Signal-In coding at $f_{CLK}/128$

8.4 Bit coding for $f_{CLK}/64$ (~212 kb/s)

8.4.1 Signal-Out

Signal-Out shall carry the XOR of the Manchester bit-coded data and the Clock, as illustrated in Figure 17.

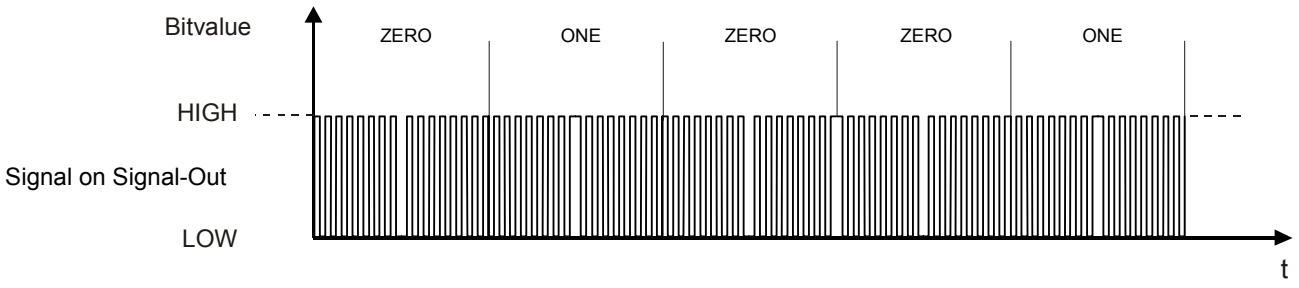

Figure 17 — Signal-Out coding at $f_{CLK}/64$

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8.4.2 Signal-In

Coding on Signal-In shall carry the Manchester bit-coded data, as illustrated in Figure 18.

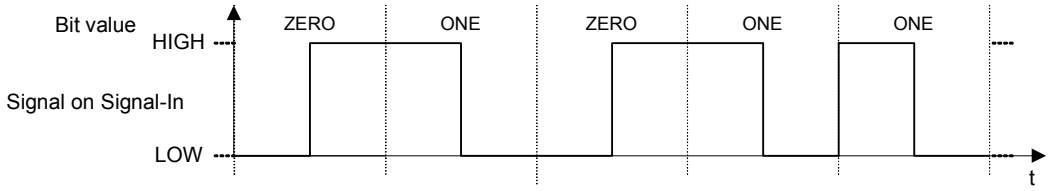

Figure 18 — Signal-In coding at $f_{CLK}/64$

8.5 Bit coding for $f_{CLK}/32$ (~424 kb/s)

The bit coding for $f_{CLK}/32$ shall be the same as the bit coding for $f_{CLK}/64$ as defined in 8.4.

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Annex A
(informative)

Application of NFC-WI with NFCIP-1

A.1 General

This Annex list specific considerations for NFCIP-1 devices that implement NFC-WI.

A.2 Reference

ISO/IEC 18092, *Information technology — Telecommunications and information exchange between systems — Near Field Communication — Interface and Protocol (NFCIP-1)*

A.3 Propagation delay

The propagation delay of the Front-end is the integer number of clock cycles needed for signal processing in the Front-end. This delay is divided into two parts, one time for Signal-Out (t_1) and one for Signal-In (t_2). The sum of them is the propagation delay.

ISO/IEC 18092 Front-ends, using the NFC-WI interface have the following requirements on the propagation delay:

For data rate $f_{CLK}/128$: ($t_1 + t_2$) equal to 128 clock cycles

For data rate $f_{CLK}/64$: ($t_1 + t_2$) maximum 256 clock cycles

For data rate $f_{CLK}/32$: ($t_1 + t_2$) maximum 256 clock cycles

A.4 Communication mode

The default communication mode is the Passive communication mode.

A.5 RF-field control during activation

In 7.2, this International Standard defines the Activating state.

The activation sequence defined in 7.2.2 only activates the NFC-WI. Whether the NFCIP-1 RF-field is switched on is described by the following two cases.

A.5.1 Activation without RF-field

When ACT_REQ_Si is shorter than 100µs the NFC-WI enters the On state without the Front-end switching on the RF-field.

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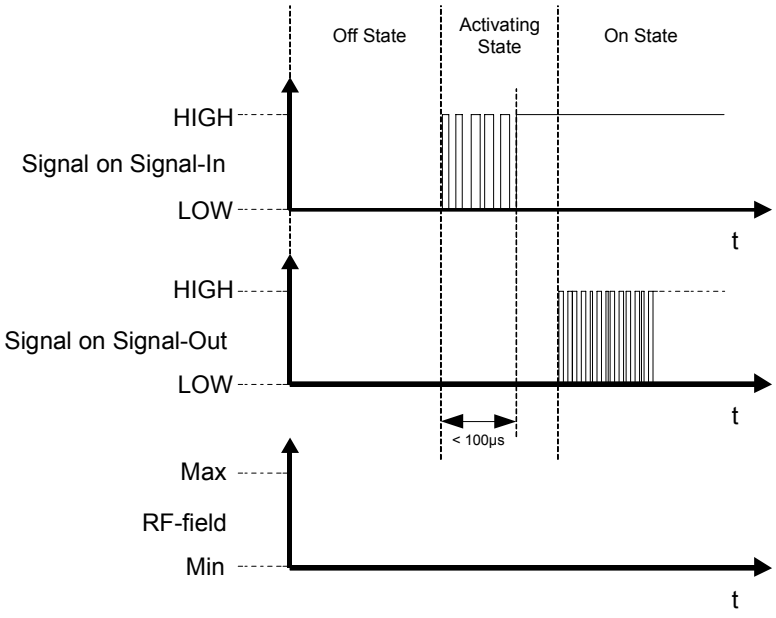

Figure A.1 — Activation without RF-field

A.5.2 Activation with RF-field

When ACT_REQ_Si is overlapping the ACT_RES_So for at least 16 clock cycles the NFC-WI enters the On state with the Front-end performing the Initial RF collision avoidance sequence as defined in ISO/IEC 18092.

If the Front-end is not able to switch on the RF-field it initiates the Signal-Out deactivation.

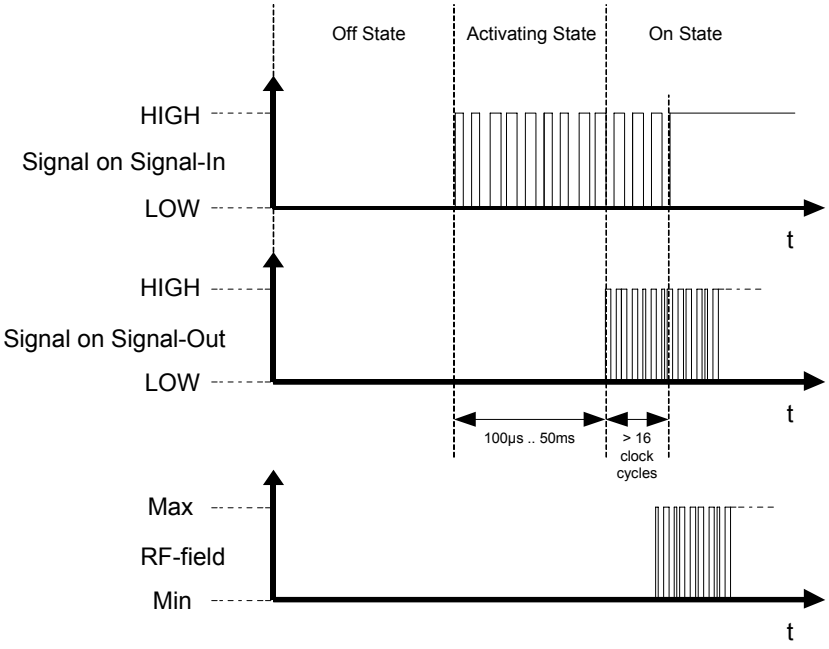

Figure A.2 — Activation with RF-field

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A.6 Signal diagrams

This Clause illustrates possible signal combinations for Signal-In, Signal-Out and the RF-field.

A.6.1 $f_{CLK}/128$

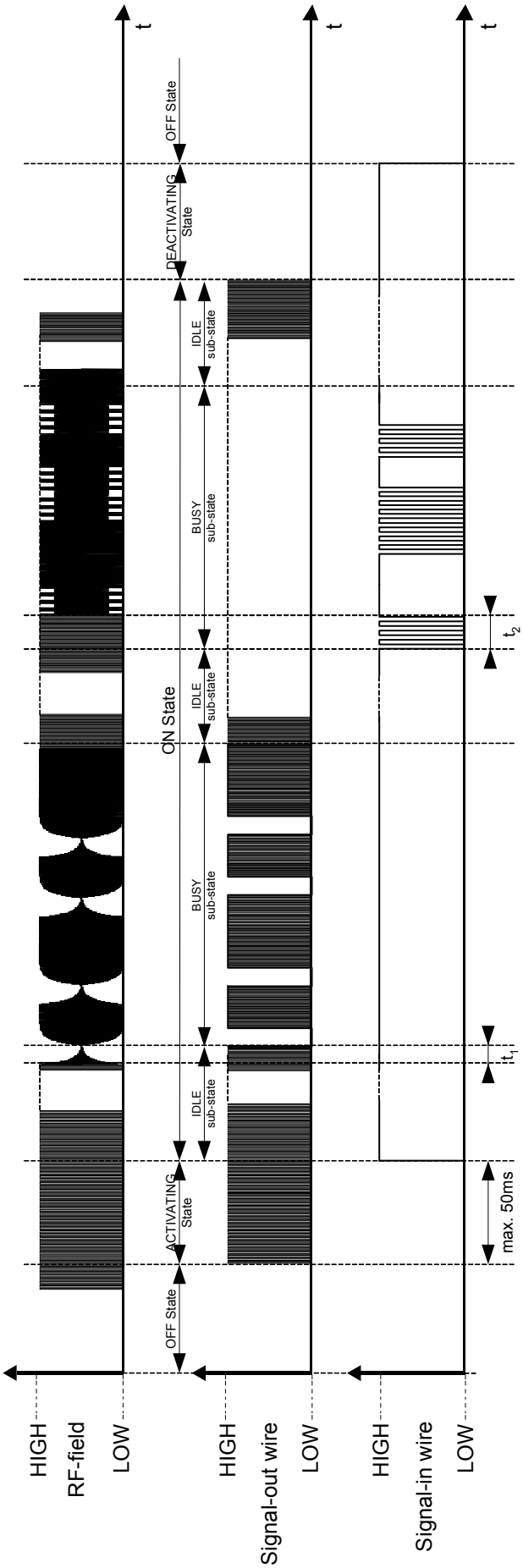

Figure A.3 —Signal diagram $f_{CLK}/128$

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A.6.2 $f_{CLK}/64$

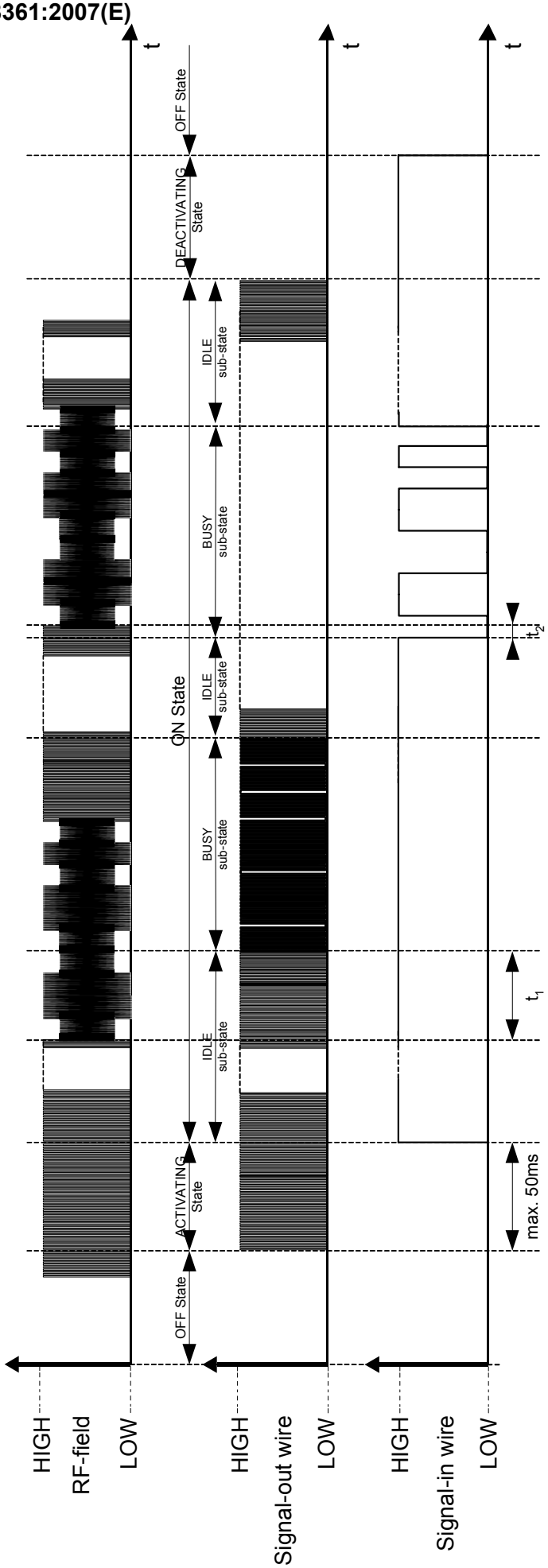

Figure A.4 — Signal diagram $f_{CLK}/64$

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Annex B
(informative)

Command state configuration

This International Standard specifies the Escape sequence to enter the Command state in 7.5. The Command state allows the exchange of control and state information between the Transceiver and the Front-end.

Such exchange may include: indication of the presence of the RF-field; information about the state of the RF-Collision avoidance; control information to change data rates and communication modes. Furthermore, the Command mode allows changing to other communication protocols.

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