

Inhaltsverzeichnis

Session 1: Testing

Using Computational Stress to Derive Stress Robustness and Timing Behaviors on Hard Real-Time Operating Systems	1
Max Brand ¹ , Albrecht Mayer ¹ and Frank Slomka ²	
¹ <i>Infineon Technologies AG</i>	
² <i>Ulm University</i>	
Towards Semantic Abstraction of Test Programs	13
Matthias Sauppe ¹ , Ulrich Heinkel ¹ and Daniel Manns ²	
¹ <i>TU Chemnitz</i>	
² <i>Presto Engineering</i>	
RVVTS: A Modular, Open-Source Framework for Positive and Negative Testing of the RISC-V 'V' Vector Extension (RVV)	20
Manfred Schlägl and Daniel Große	
<i>Johannes Kepler University, Linz</i>	

Session 2: Virtual Prototyping and Simulation

Symbolic Execution of Unmodified SystemC Peripherals	23
Karl Aaron Rudkowski, Sallar Ahmadi-Pour and Rolf Drechsler	
<i>University of Bremen</i>	
Minimizing simulation effort during temporal distribution analysis in real-time systems	27
Andre Gaschler and Frank Slomka	
<i>Ulm University</i>	
Verilator and FireSim RTL Simulations on a HPC Cluster: A Comparative Case Study	35
Kai Arne Hannemann, Hüseyin Berke Bütün, Wolfgang Mueller and Christoph J. Scheytt	
<i>Paderborn University</i>	
Towards Non-Intrusive SystemC Checkpointing for Digital Virtual Prototypes.....	41
Deepak Ravibabu ¹ , Muhammad Hassan ¹ , Thilo Vörtler ² , Karsten Einwich ² , Rolf Drechsler ³ and Daniel Große ⁴	
¹ <i>Cyber-Physical Systems, DFKI GmbH</i>	
² <i>COSEDA Technologies GmbH</i>	
³ <i>University of Bremen</i>	
⁴ <i>Johannes Kepler University, Linz</i>	

Session 3: Architectures and System Modeling

Latency-Constrained Neural Architecture Search for U-Nets on Graphics Processing Units.....	52
Stefan Groth ¹ , Christian Heidorn ¹ , Moritz Schmid ² , Jürgen Teich ¹ and Frank Hannig ¹	
¹ <i>Friedrich-Alexander-Universität Erlangen-Nürnberg</i>	
² <i>Siemens Healthineers</i>	

Design Exploration für RISC-V Prozessoren zur Optimierung von Erklärbarkeit für Maschinelles Lernen	61
Johannes Rust, Rolf Drechsler and Serge Autexier	
<i>DFKI Bremen</i>	
Improving Design Generation by Interface Configuration Propagation.....	65
Natalie Simson, Paritosh Kumar Sinha and Wolfgang Ecker	
<i>Infineon Technologies AG</i>	
Exploration of Clock and Power Gating Tradeoffs for the Design of Self-Powering Dataflow Networks	73
Abrarul Karim, Joachim Falk and Jürgen Teich	
<i>Friedrich-Alexander-Universität Erlangen-Nürnberg</i>	
Platform-Aware RTL Generation: Bridging the Gap between Design and Implementation	83
Mohamed Badawy ^{1,2} , Nicolas Gerlin ¹ , Paritosh Kumar Sinha ¹ , Endri Kaja ¹ , Jad Al Halabi ¹ , Stephanie Ecker ^{1,3} , Natalie Simson ^{1,2} and Wolfgang Ecker ^{1,2}	
¹ <i>Infineon Technologies AG</i>	
² <i>Technical University of Munich</i>	
³ <i>CHIPGLOBE GmbH</i>	

Session 4: Specification and Code Generation

Enhancing LLM-Generated Hardware Documentation: Post-Processing and Prompt Engineering Techniques.....	90
Robert Kunzelmann ^{1,2} , Saruni Fernando ^{1,3} and Wolfgang Ecker ¹	
¹ <i>Infineon Technologies AG</i>	
² <i>Technical University of Munich</i>	
³ <i>Rosenheim Technical University of Applied Sciences</i>	
Erfassung und Austausch prozessspezifischer Anforderungen entlang der Wertschöpfungskette.....	98
Franziska Mayer, Christian Schott, Davis John Chellappa, Erik Markert and Ulrich Heinkel	
<i>Technical University of Chemnitz</i>	
Rustifying Embedded Software Development: A Model-Based Code Generation Approach for Auto-Generation of C and RUST	105
Raphael Kunz ^{1,2} , Mayuri Bhadra ^{1,2} , Stephanie Ecker ^{1,2,3} and Wolfgang Ecker ^{1,2}	
¹ <i>Infineon Technologies AG</i>	
² <i>Technical University of Munich</i>	
³ <i>CHIPGLOBE GmbH</i>	
Parameterized Construction and Constraint-Driven Validation of Formal Hardware Specifications for Efficient Code Generation	113
Robert Kunzelmann ^{1,2} , Maximilian Berger ^{1,2} and Wolfgang Ecker ¹	
¹ <i>Infineon Technologies AG</i>	
² <i>Technical University of Munich</i>	

Session 5: Formal Verification and Security

VeriCHERI: Exhaustive Formal Security Verification of CHERI at the RTL.....	122
Anna Lena Duque Antón ¹ , Johannes Müller ¹ , Philipp Schmitz ¹ , Tobias Jauch ¹ , Alex Wezel ¹ , Lucas Deutschmann ¹ , Mohammad Rahmani Fadiheh ² , Dominik Stoffel ¹ and Wolfgang Kunz ¹	
¹ <i>RPTU Kaiserslautern-Landau</i>	
² <i>Stanford University</i>	
Hardware Trojan Detection using Formal Verification and Automation.....	126
Czea Sie Chuah ¹ , Christian Appold ² and Tim Leinmüller ²	
¹ <i>Technical University of Munich</i>	
² <i>DENSO AUTOMOTIVE Deutschland GmbH</i>	
Coverage Metrics for Security Property Verification: A Novel Approach.....	130
Jaimini Nagar ¹ , Thorsten Dworzak ¹ , Sebastian Simon ¹ , Ulrich Heinkel ² and Djones Lettnin ¹	
¹ <i>Infineon Technologies AG</i>	
² <i>Technical University of Chemnitz</i>	
Embedding Modulo Counter Circuits for their Polynomial Formal Verification.....	138
Caroline Dominik and Rolf Drechsler	
<i>University of Bremen, Germany</i>	

Session 6: System Analysis

Data-Driven Probabilistic Evaluation of Logic Properties with PAC-Confidence on Mealy Machines.....	142
Swantje Plambeck ¹ , Ali Salamati ² , Eyke Hüllermeier ² and Goerschwin Fey ¹	
¹ <i>Hamburg University of Technology</i>	
² <i>Ludwig Maximilian University Munich</i>	
Dead-Code Detection with IC3 using SMT-LIBv2 Solvers.....	150
Lukas Mentel ¹ , Tobias Seufert ² , Karsten Scheibler ¹ and Christoph Scholl ²	
¹ <i>BTC Embedded Systems AG</i>	
² <i>University of Freiburg</i>	
Efficient Hierarchical Decomposition of Repetitive Traces for ML-Driven Analysis.....	160
Johannes KnödteI and Marc Reichenbach	
<i>University of Rostock</i>	
Information Flow Analysis - Understanding the Trade-Offs between Static and Dynamic Analysis	169
Lutz Schammer, Gianluca Martino and Goerschwin Fey	
<i>Hamburg University of Technology</i>	

Demo

Open-Source Software for Heaviside Real-Time Analysis.....	173
Iwan Feras Fattohi ¹ , Christian Prehofer ² and Frank Slomka ¹	
¹ <i>Ulm University</i>	
² <i>Technical University of Munich</i>	